CMOS IC

LC573718A

4-Bit Microcontroller with 8K-Byte ROM, 512 × 4 bits RAM and LCD

UnderDevelopment

Overview

The LC573718A is a CMOS 4-bit microcontroller that operates on low voltage and very low power consumption. It also contains 8K-byte ROM, 512 × 4 bits RAM, LCD drivers and 1/100sec. chronograph function.

Features

(1) ROM: 8192 × 8 bits

(2) RAM: 512 × 4 bits

(3) Cycle Time

122μs: VDD = 2.4V to 3.6V

(4) Input / Output Terminals

- Input / Output ports: 6 terminals
- Input ports: 6 terminals (S-port : 4 terminals, M-port : 2 terminals)
- LCD common output ports: 4 terminals
- LCD segment output ports: 32 terminals

(CMOS/P-ch OD can be switched by mask option.: 16 terminals (SEG17-SEG32))

SANYO Electric Co.,Ltd. Semiconductor Company

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(5) LCD driver

- Display duty: 1/3, 1/4 duty
- Display bias: 1/2, 1/3 bias
- Built-in step-up / step-down circuit
- LCD driver

Segment output terminals: (32-N) terminals
(N: the number of output terminals specified by mask option)
Common output terminals: 4 terminals

(6) Buzzer output

- 2kHz/4kHz buzzer output is possible.
- Modulation output is possible.

(7) Base timer

- Generates an overflow every 500ms for a clock application.

(8) 1/100sec. chronograph function

- Start/stop/lap: Handled by software program

(9) HALT release

- Five vectors
  1. 15-bit base timer (500ms overflow output)
  2. 15-bit base timer (output every 32ms)
  3. S-port
  4. M-port
  5. 1/10 sec. pulse

(10) Stand-by mode

- HALT mode

The program operation will be stopped in this mode. This mode is released by system reset or the triggering of any of the 5 vectors for HALT release mentioned above.

(11) System reset

- RES terminal

(12) Oscillation

32.768kHz crystal oscillation
Capacitor on output side (XT2) must be connected externally.
Capacitor in input side (XT1) must be connected externally.

(13) Power supply

- VDD2 = 2.4V to 3.6V
- VDD1 = 1.2V to 1.8V, VDD3 = 3.6V to 5.4V (LCD power supply)

(14) Shipping form

- Chip

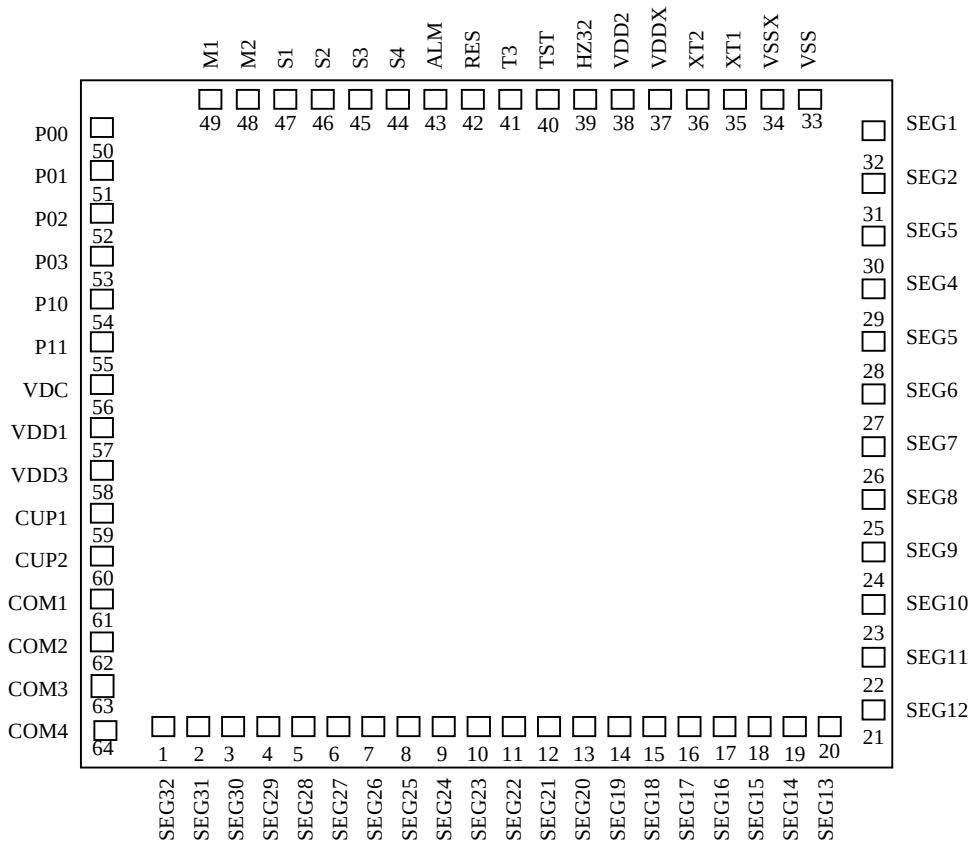
(15) The development tool

- Emulator: TB - 573718 (Include EVA57)

Pad Assignment

Pad pitch: 110μm

Pad size: 80μm (Jacket open space)

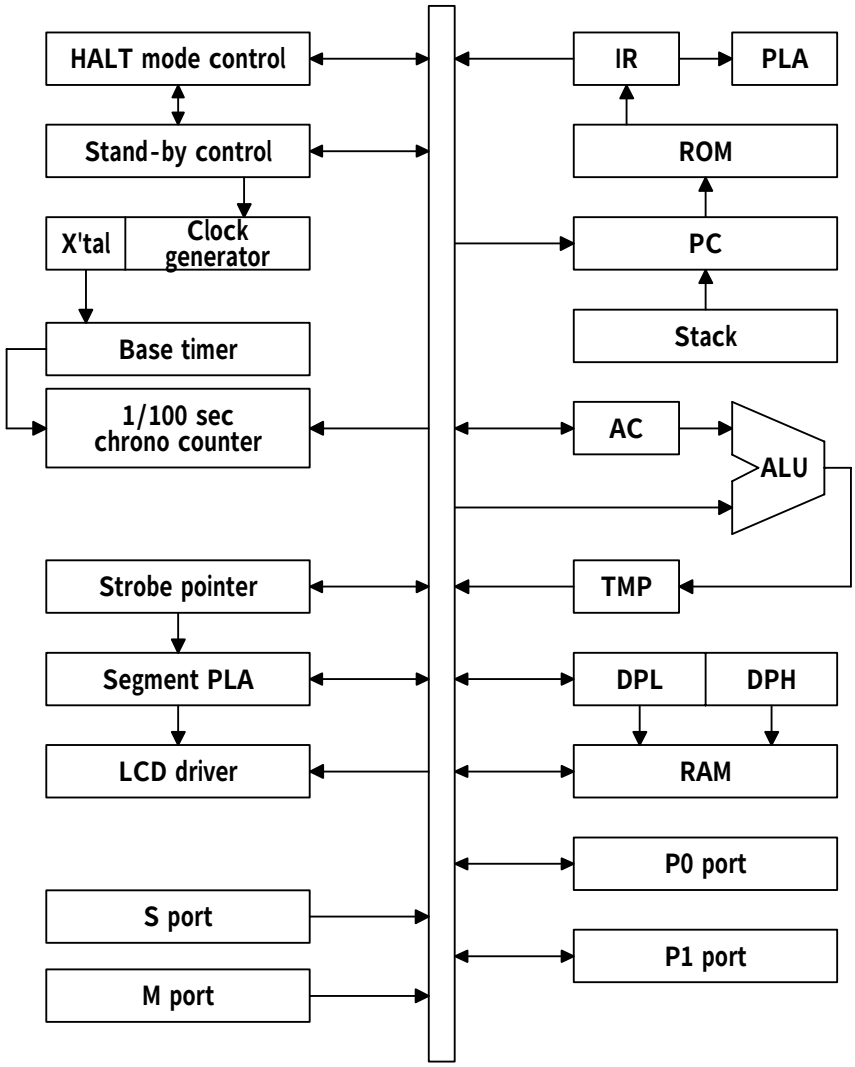


Pin Name and Coordinates

Pad No.	Pad Name	Coordinates		Pad No.	Pad Name	Coordinates	
		Xμm	Yμm			Xμm	Yμm
1	SEG32	-987	-1365	33	VSS	1066	1365
2	SEG31	-877	-1365	34	VSSX	936	1365
3	SEG30	-767	-1365	35	XT1	826	1365
4	SEG29	-657	-1365	36	XT2	716	1365
5	SEG28	-547	-1365	37	VDDX	606	1365
6	SEG27	-437	-1365	38	VDD2	456	1365
7	SEG26	-327	-1365	39	HZ32	346	1365
8	SEG25	-217	-1365	40	TST	236	1365
9	SEG24	-107	-1365	41	T3	126	1365
10	SEG23	3	-1365	42	RES	16	1365
11	SEG22	113	-1365	43	ALM	-114	1365
12	SEG21	223	-1365	44	S4	-224	1365
13	SEG20	333	-1365	45	S3	-334	1365
14	SEG19	443	-1365	46	S2	-444	1365
15	SEG18	553	-1365	47	S1	-554	1365
16	SEG17	663	-1365	48	M2	-664	1365
17	SEG16	773	-1365	49	M1	-774	1365
18	SEG15	883	-1365	50	P00	-1297	1228
19	SEG14	993	-1365	51	P01	-1297	997
20	SEG13	1103	-1365	52	P02	-1297	766
21	SEG12	1297	-1330	53	P03	-1297	535
22	SEG11	1297	-1098	54	P10	-1297	304
23	SEG10	1297	-867	55	P11	-1297	73
24	SEG09	1297	-635	56	VDC	-1297	-158
25	SEG08	1297	-404	57	VDD1	-1297	-390
26	SEG07	1297	-172	58	VDD3	-1297	-620
27	SEG06	1297	59	59	CUP1	-1255	-834
28	SEG05	1297	290	60	CUP2	-1255	-944
29	SEG04	1297	522	61	COM1	-1255	-1054
30	SEG03	1297	753	62	COM2	-1255	-1164
31	SEG02	1297	984	63	COM3	-1255	-1274
32	SEG01	1297	1216	64	COM4	-1255	-1384

The pad coordinates are such that the chip center is taken as the origin and the values for (X, Y) represent the coordinates of the center point of each pad.

System Block Diagram



LC573718A Terminal Description

Name	Pin No.	I/O	Function Description	Option
VSS,VSSX	33, 34	-	Power terminal (–)	-
VDDX,VDD2	37, 38	-	Power terminal (+)	-
CUP1	59	-	Capacitor connecting terminals for step-up/stop down	-
CUP2	60	-	Capacitor connecting terminals for step-up/stop down	
VDD1,VDD3	57, 58	-	Power supply for driving LCD	-
VDC	56	-	Power supply for internal logic circuit	-
P0 P00 - P03	50-53	I/O	•4-bit I/O port •I/O programmable in port unit •In input mode, built-in pull-up resistor: ON •While in output mode with P-ch OD selected, a built-in circuit inhibits the input terminal from floating.	Output form CMOS/ Pch-OD **(*Note 1*)**
P1 P10 - P11	54,55	I/O	•2-bit I/O port •I/O programmable in port unit •In input mode, built-in pull-up resistor: ON •While in output mode with P-ch OD selected, a built-in circuit inhibits the input terminal from floating.	Output form CMOS/ Pch-OD **(*Note 1*)**
S port S1 - S4	47 - 44	I	•4-bit input port •Input for HALT release •Built-in programmable pull-down resistor	
M port M1 - M2	49, 48	I	•2-bit input port •Input for HALT release •Built-in programmable pull-down resistor	
ALM	43	O	•Output port •Alarm output only terminal •4kHz and 2kHz signals output by instructions SAS and TMEL	
COM1 - COM4	61 - 64	O	LCD output terminals for common	-
SEG1 – SEG32	32 - 1	O	LCD output terminals for segment	SEG1-SEG32:Segment PLA SEG17-SEG32 Output from:Segment/CMOS/P-ch open drain
RES	42	I	•Reset •Built-in pull-down resistor	-
T3	41	O	•Test terminal •This terminal should be left unconnected.	-
HZ32	39	-	•Test terminal •This terminal should be left unconnected.	-
XT1	35	I	Input for 32.768kHz crystal oscillation	-
XT2	36	O	Output for 32.768kHz crystal oscillation	-

Note 1: P-ch OD: P channel open drain

Port's option is specified for each port individually.

* A state of port at initial

Name	I/O	Pull-up / Pull-down Resistor Status
P0, 1	I	Pull-up resistor
S, M_PORT	I	Programmable pull-down resistor ON

Name	Output Level
COM1-COM4	VSS (display OFF)
SEG1-SEG32	VSS (display OFF)

1. Absolute Maximum Ratings / Ta = 25°C, VSS = 0V

Parameter		Symbol	Pins	Conditions		Limits			
					VDD[V]	Min.	Typ.	Max.	Unit
Supply voltage		VDDMAX	VDD2			-0.3	-	+4.0	V
Input voltage		VI(1)	Ports S, M, RES			-0.3	-	VDD+0.3	
Output voltage		VO(1)	C1-C4, S1-S32 CUP1 (1/3 bias)			-0.3	-	3/2VDD +0.3	
		VO(2)	C1-C4, S1-S32 CUP1 (1/2 bias) CUP2, ALM			-0.3	-	VDD+0.3	
I/O voltage		VIO(1)	Ports 0, 1			-0.3	-	VDD+0.3	
High level output current	Peak output current	IOPH(1)	• Ports 0, 1 • S17-S32 (CMOS, P-ch OD) • ALM	For each pin		-1			mA
	Total output current	ΣIOAH(1)	• Ports 0, 1 • C1-C4, S1-S32 • ALM	The total of all pins		-10			
Low level output current	Peak output current	IOPL(1)	• Ports 0, 1 • S17-S32 (CMOS) • ALM	For each pin				1	
	Total output current	ΣIOAL(1)	• Ports 0, 1 • C1-C4, S1-S32 • ALM	The total of all pins.				10	
Operating temperature range		Topg				-30	-	70	°C
Storage temperature range		Tstg				-40	-	125	

2. Recommended Operating Range / Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	Min.	Typ.	Max.	Unit
Operating supply voltage range	VDD(1)	VDD2			2.4		3.6	V
Hold voltage	VHD	VDC	RAM's and the register's data are kept in HOLD mode.		1.2		3.6	
Supply voltage for LCD	VSUP	VDD3	1/2 bias	2.4 - 3.6	0		VDD	
			1/3 bias	2.4 - 3.6	0		3/2VDD	
High level input voltage	VIH(1)	Ports 0, 1	Input mode	2.4 - 3.6	0.7VDD		VDD	
	VIH(2)	Ports S, M		2.4 - 3.6	0.7VDD		VDD	
	VIH(3)	RES (Schumitt)		2.4 - 3.6	0.7VDD		VDD	
Low level input voltage	VIL(1)	Ports 0, 1	Input mode	2.4 - 3.6	VSS		0.15VDD	
	VIL(2)	Ports S, M		2.4 - 3.6	VSS		0.15VDD	
	VIL(3)	RES (Schumitt)		2.4 - 3.6	VSS		0.15VDD	
Operation cycle time	Tcyc			2.4 - 3.6		122		µs
Oscillation frequency range (***Note 2***)	FXtal	XT1, XT2	32.768kHz crystal oscillation Refer to Fig. 1	2.4 - 3.6	32	32.768	33	kHz

Note 2: Refer to Table 1 about oscillation constant.

3. Electrical Characteristics / Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits Min.	Typ.	Max.	Unit
High level input current	IIH(1)	Ports S, M	Programmable pull-down Tr OFF, VIN=VDD	2.4 - 3.6			1	μA
Low level input current	IIL(1)	Ports S, M	Programmable pull-down Tr OFF, VIN=VSS	2.4 - 3.6	-1			V
High level output voltage	VOH(1)	Ports 0, 1, ALM	IOH=-200μA	2.4 - 3.6	VDD-0.2			
	VOH(2)	CMOS, P-ch OD of SEG17-SEG32	IOH=-100μA	2.4 - 3.6	VDD-0.2			
	VOH(3)	SEG1-SEG32 (LCD driver)	IOH=-0.4μA 1/2 bias	2.4 - 3.6	VDD-0.2			
	VOH(4)	SEG1-SEG32 (LCD driver)	IOH=-0.4μA 1/3 bias	2.4 - 3.6	3/2VDD -0.2			
	VOH(5)	COM1-COM4	IOH=-4μA 1/2 bias	2.4 - 3.6	VDD-0.2			
	VOH(6)	COM1-COM4	IOH=-4μA 1/3 bias	2.4 - 3.6	3/2VDD -0.2			
Middle level output voltage	VOM(1)	SEG1-SEG32 (LCD driver)	IOL=0.4μA, IOH=-0.4μA 1/3 bias	2.4 - 3.6	VDD-0.2		VDD+0.2	
	VOM(2)	SEG1-SEG32 (LCD driver)	IOL=0.4μA, IOH=-0.4μA 1/3 bias	2.4 - 3.6	1/2VDD -0.2		1/2VDD+ 0.2	
	VOM(3)	COM1-COM4	IOL=4μA, IOH=-4μA	2.4 - 3.6	1/2VDD -0.2		1/2VDD+ 0.2	
	VOM(4)	COM1-COM4	IOL=4μA, IOH=-4μA 1/3 bias	2.4 - 3.6	VDD-0.2		VDD+0.2	
Low level output voltage	VOL(1)	CMOS output of ports 0, 1, ALM	IOL=200μA	2.4 - 3.6			0.2	
	VOL(2)	CMOS output of SEG17-SEG32	IOL=100μA	2.4 - 3.6			0.2	
	VOL(3)	SEG1-SEG32 (LCD driver)	IOL=0.4μA	2.4 - 3.6			0.2	
	VOL(4)	COM1-COM4	IOL=4μA	2.4 - 3.6			0.2	
Pull-up resistor	Rpu	Ports 0, 1	VIN=0.9VDD	2.4 - 3.6	25	50	150	kΩ
Pull-down resistor	Rpd	Ports S, M	VIN=0.1VDD	2.4 - 3.6	50	100	300	
Hysteresis voltage	VHIS	Ports 0, 1 RES	Output disable	2.4 - 3.6		0.1VDD		V
Pin capacitance	CP	All pins	f=1MHz All pins except the measured terminal: VIN=VSS Ta=25°C	2.4 - 3.6		10		pF

4. Pulse Input Condition / Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pin	Condition	Limit				
				VDD[V]	Min.	Typ.	Max.	Unit
High/low level pulse width	tPIL(4)	RES	Reset acceptable	2.4 - 3.6	10			μs

5. Sample Current Dissipation Characteristics / Ta=-30°C to + 70°C, VSS=0V

The sample current dissipation characteristics are the measurement result of Sanyo provided evaluation board. The currents though the output transistor and the pull-up or pull-down MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	Min.	Typ.	Max.	Unit
Current dissipation	IDDOP (during normal operation)	VDD	Ta ≦ 50°C 32.768kHz crystal oscillation Refer to Figure 2. (typ=3.0V)	2.4 - 3.6		1.5	5	μA
	IDDHALT (in HALT mode)					0.6	3	

6. LCD Power Voltage Characteristics / Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins and conditions	Limits				Unit
			VDD[V]	Min.	Typ.	Max.	
VDD1 output voltage	VDD1	LCD ON	2.9	0.45VDD	0.50VDD	0.55VDD	V
VDD3 output voltage	VDD3	1/3 bias Refer to Figure 2.	2.9	1.45VDD	1.50VDD	1.55VDD	

Table 1 Crystal Oscillation Recommended Constant

Frequency	Manufacturer	Oscillator	C1
32.768 kHz Xtal oscillation	CITIZEN	CFS-308	?pF
	SEIKO	DT-VT-200	?pF

(C1 must meet J level tolerances (±5%) or if high accuracy is not required, then C1 must meet K level tolerances (±10%) and SL characteristics.)

Notes:

- *Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.*
- *If you use other oscillators herein, we provide no guarantee for the characteristics*

Recommended Oscillation Circuit and Characteristics

The oscillation circuit characteristics in the table below are based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- The characteristics are the results of the evaluation with the recommended circuit parameters connected externally.

Recommended Oscillation Circuit Parameters and Characteristics (Ta = 0°C to +50°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameter	Operating supply voltage range	Oscillation stabilizing time (*)	
					Typ.	Max.
32.768kHz	SII	DT-VT-200	C1=?pF	2.4V - 3.6V	TssX'tal	
					1.00s	3.00s
	CITIZEN WATCH CO., LTD.	CFS-308	C1=?pF	2.4V - 3.6V	TssX'tal	
					1.00s	3.00s

(*) Note: The oscillation stabilizing time period is the time until the oscillation becomes stable after the VDD becomes higher than the minimum operating voltage.

The oscillation circuit characteristics may differ by applications. For further assistance, please contact with the oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.

Since the oscillation circuit characteristics are affected by the noise, wiring capacity, etc., refer to the following notices.

- The distance between the clock I/O terminal and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or the signal line with large amplitude such as middle withstand voltage port or LCD driver output should be allocated away from the clock oscillation circuit.
- The signal lines with large current should be allocated away from the oscillation circuit.

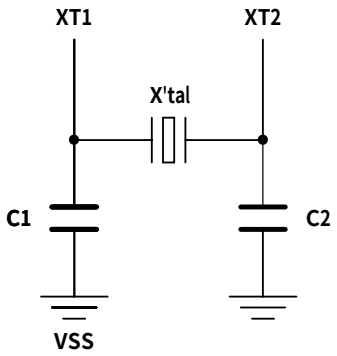


Figure 1 Crystal Oscillation Circuit

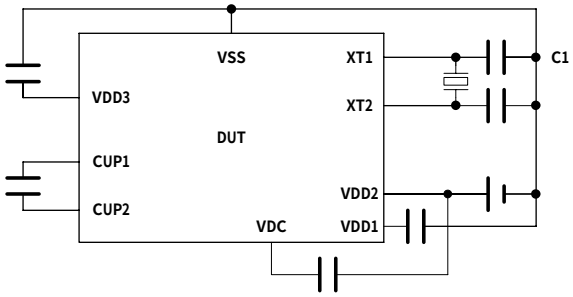


Figure 2 Current Dissipation Measurement Circuit/VDD1 and VDD3 Terminals Output Voltage Measurement Circuit (1/3 Bias)

Note:

The specification above indicates the operational characteristics of a die that has been packaged by SANYO into a QIC64 package. If you purchase this product in die form and use a third party to package the die, then please note that the operational characteristics may vary depending on the packaging techniques that are used.